IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:)
MIRABEL ET AL.)
)
Serial No. **10/616,413**)
)
Filing Date: **July 9, 2003**)
)
For: **METHOD OF CONTROLLING AN**)
ELECTRONIC NON-VOLATILE MEMORY)
AND ASSOCIATED DEVICE)
)

CITATION UNDER 37 CFR §1.97

COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

Sir:

Attached is Form PTO-1449 listing several references for consideration in the examination of the above-identified application. A copy of each reference is also enclosed. It is requested that these references be considered by the Examiner and officially made of record in accordance with the provisions of 37 CFR §1.97 and Section 609 of the MPEP.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, on this 6th day of August, 2003.

INFORMATION DISCLOSURE STATEMENT	Atty Docket:	02RO18854478
	Serial No.:	10/616,413
	Applicant:	MIRABEL ET AL.
	Filing Date:	July 9, 2003
	Group:	

U.S. PATENT DOCUMENTS

Examiner Initials		Document Number	Date	Name	Class	Sub Class	Filing Date
	AA	5,726,933	3/10/98	Lee et al.	365	185.18	
	AB	5,781,477	7/14/98	Rinerson et al.	365	185.29	
	AC	5,790,460	8/4/98	Chen et al.	365	185.29	
	AD	5,933,367	8/3/99	Matsuo et al.	365	185.29	
	AE	6,236,596	5/22/01	Sobek et al.	365	185.27	
	AF						
	AG						
	AH						

FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Sub Class	Translation
	AI						
	AJ						
	AK						
	AL						

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AM	Laffont et al., *Decreasing EEPROM Programming Bias with Negative Voltage Reliability Impact*, IEEE International Workshop on Memory Technology, Design and Testing (MTDT 2002), July 10, 2002, Pages 168-173, XP010601068
	AN	Benzerti et al., *Effect of the Selection MOS Transistor Polarization Voltage During a Write and an Erase Operation of an EEPROM Memory Cell*, Microelectronics, 1998, ICM 98, Proceedings of the Tenth International Conference on Monastir, Tunisia, December 14-16, 1998, Piscataway, NJ, US, December 14, 1998, Pages 149-152, XP010371938
	AO	

EXAMINER:	DATE CONSIDERED:

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.